6800-6809 MOTHER BOARD

Introduction

The GIMIX GHOST MOTHER BOARD provides bus interconnections and physical support for the other boards in the GIMIX GHOST computer. It has 15 slots for full-sized (SS-50) boards, and 8 slots for I/O-sized (SS-30) boards.

The board has many features which make it very versatile and easy to use in a variety of applications and configurations.

ITS MAIN FEATURES ARE:

* Fully compatible with the SS-50 (6800) and SS-50C (6809) buses.
* Gold bus connectors
* 4, 8, or 16 decoded addresses per I/O slot
* On board baud rate generator (75 to 38,400 baud)
* All data an address buffers have hysteresis for increased noise margins.
* The I/O block is DIP-switch addressable to any 32, 64, or 128 byte boundary (depending on the selected number of addresses per slot).

HARDWARE CONFIGURATION:

I/O SLOT SIZE:

There are two ways to change the I/O slot size depending on the users needs. The board is normally supplied with 1 74LS244 IC. installed at location U-3 and DIP-switch S3-1 ON. This selects 4 decoded addresses per I/O slot. To select either 8 or 16 addresses per slot move the 74LS244 to location U-4 (8 addresses) or U-5 (16 addresses) and set the corresponding section of SW-3 ON (S3-2 for 8 and S3-3 for 16).

If you wish to be able to change I/O slot size by DIP-switch alone without moving the 74LS244 you can install additional 74LS244s at locations U-4 and U-5 and turn on the proper switch section for the desired slot size. NOTE: BE SURE ONLY THE DIP-SWITCH SECTION CORRESPONDING TO THE DESIRED SLOT SIZE IS ON, THE OTHER 2 OF THE 3 SECTIONS (S3-1,2,3,) THAT CONTROL SLOT SIZE MUST BE OFF.

Regardless of the method selected for determining I/O slot size, when using 8 addresses per slot, S1-1 (A5) is a "DON'T CARE", its position does not affect the address decoding. When using 16 addresses per slot, S1-1 (A5) and S1-2 (A6) MUST BE IN THE ON POSITION for correct decoding.

I/O BLOCK ADDRESSING:

THE DIP-switches S-1 and S-2 control the addressing of the I/O block The I/O block occupies 32, 64, or 128 bytes depending on whether you are using 4, 8, or 16 addresses per I/O slot. S2-6 enables and disables the entire block. When S2-6 is ON the I/O block is disabled and no decoding takes place. With S2-6 OFF the I/O block is enabled and it appears beginning at the addresss set by the remaining sections of switches S-1 and S-2.

S1 section 1 thru 6 correspond to address bits 5 thru 10, and S2 sections 1 thru 5 correspond to address bits 11 thru 15 respectively When a switch is ON the corresponding address bit must be a 0 for a match. When a switch is OFF that address bit must be a 1 for a match. Thus a switch setting of ON,OFF,ON,OFF,ON,ON,OFF,OFF is equivalent to a binary address of 01010011 .

ADDRESSING EXAMPLES:

I/O block at $8000 (standard MIKBUG<R> location).

```
    S1                          S2
1 2 3 4 5 6                 1 2 3 4 5 6
                                                S3-1 = ON (closed)
0 0 0 0 0 0                 0 0 0 0 0 0         74LS244 at location
N N N N N N                 N N N N F F         U-3 for 4 addresses
                                        F F     per slot.
```

I/O block at $F400 (8 addresses per slot).

```
    S1                          S2
1 2 3 4 5 6                 1 2 3 4 5 6
                                                S3-2 = ON (closed)
X 0 0 0 0 0                 0 0 0 0 0 0         74LS244 at location
  N N N N F                 N F F F F F         U-4 for 8 addresses
          F                   F F F F F         per slot.
```

X="DON'T CARE"

I/O block at $E000 (16 addresses per slot).
(standard GMXBUG09 / SBUG-E location)

```
    S1                          S2
1 2 3 4 5 6                 1 2 3 4 5 6
                                                S3-3 = ON (closed)
0 0 0 0 0 0                 0 0 0 0 0 0         74LS244 at location
N N N N N N                 N N F F F F         U-5 for 16 addresses
* *                                F F F F     per slot.
```

*="MUST BE ON"
(For 16 addresses per slot)

BAUD RATE SELECTION:

Note: All references to baud rates assume a UART or ACIA which requires or is programmed for a 16X clock input.

The baud rate generator provides 17 standard baud rates from 75 to 38,400 baud. The baud rates are divided into two groups, the low group from 75 to 9600 baud and the high group from 300 to 38,400 baud. DIP-switch S3-6 (B) selects which group is available at the DIP-socket / header at location J-1. When S3-6 is ON (closed) the low group is selected, when S3-6(B) is OFF(open) the high group is selected. Up to 5 different rates from the selected group can be connected to the 5 baud rate lines of the 30 pin I/O bus by jumpers on the header at J-1 . Pins 10 thru 14 of the header connect to the buffer that drives the I/O bus lines. Pins 1 thru 9 connect to the outputs of the 14411 bit rate generator IC U-13.

The baud rates shown on the schematic diagram are those available when the low group is selected. When the high group is selected the available rates are four times those shown in the diagram.

The following are the available baud rates and their corresponding pins at J-1 for both the low (L) and high (H) groups.

PIN #	L	H	PIN #	L	H
1	1200	4800	6	75	300
2	600	2400	7	2400	9600
3	300	1200	8	9600	38400
4	150	600	9	4800	19200
5	110	*			

* 4 times 110 baud produces a non standard rate.

Normally the GIMIX MOTHER BOARD is supplied with the header jumpered for the standard 110 thru 1200 baud lines. To change any of these remove the jumper from the desired input and connect a new jumper from the desired output line to that input. The board comes with either of two types of header. One is a standard solder type header. Old jumpers can be unsoldered and new ones soldered in. The other type which may be supplied is an insulation displacement header. Remove the old jumpers by carefully pulling them up with a needle-nose pliers. New ones must be made from #26 or #27 Ga. magnet wire . Press the end of the wire carefully into the notched contact of the header with the needle-nose pliers. A length of the proper wire for the jumpers is provided with boards that have this type of header.

In addition a second jumper area has been provided to allow the interconnection of the baud rate lines of the 30 pin I/O bus and the corresponding lines of the main bus. When boards such as the GIMIX 8 port serial board without on board baud rate generator are to be used, one or more jumpers must be installed at this location to provide baud rates. This jumper area is located at the left rear corner of the 50 pin bus and consists of two rows of five gold plated pins which can be strapped as required with wire wrap or with standard 0.100 center jumper blocks.

SWTPC MF-68 DISK SYSTEMS:

For the convienience of those using the SWT MF-68 disk system S3-4(D) has been included. Setting this switch ON connects the select line of I/O slot #5 to UD-3 as required by this disk system. Unless an MF-68 system is being used this switch should be OFF.

6809 SLOW I/O CIRCUIT:

The GIMIX mother board includes a slow I/O device circuit for use with 6809 CPU based systems. This circuit allows the use of slower I/O devices with higher speed versions of the 6809. The circuit generates a pulse, of controlled duration each time the I/O bus is accessed by the CPU. When S3-5(S) is ON the output is connected to the MRDY line on the bus and a slow memory cycle is generated when the I/O bus is accessed.

ADDITIONAL JUMPER PADS:

Jumper pads N thru R (see schematic and board layout diagrams) allow rearranging the connections between the main bus interrupt lines (NMI, IRQ, and UD2 < 6809 FIRQ >) and the I/O bus. To rearrange these connections cut the PC traces ,If any, between the pads and solder jumpers between them as required.

EXTERNAL CONNECTIONS:

Two clamping terminal blocks, one at the front and one at the rear of the board, are provided for making external connections to the buses. The one at the front provides the following connections

1	2	3	4	5	6	7	8	9	10	11	12	13	14
Q	F I R Q	*	M R D Y	+ 1 6 V	- 1 6 V	+ 8 V	+ 8 V	+ 8 V	G N D	G N D	G N D	G N D	G N D

* = no connection tie point only

The rear terminal block provides the following connections.

1	UD1
2	UD2
3	UD3
4	UD4

NOTE: SOME OF THESE LINES MAY HAVE DIFFERENT SIGNALS DEPENDING ON THE BUS DEFINITION BEING USED (SS-50 or SS-50C) SEE THE CHART AT THE END OF THIS MANUAL FOR FURTHER DETAILS.

HARDWARE DESCRIPTION:

I/O DECODING:

U-2 (74LS240) and U-3, U-4,or U-5 (74LS244) provide buffering for the address and control signals from the main bus. The position of the 74LS244 at either U-3,4,or 5 determines how the address lines connect to the decoding circuitry and therefore how many addresses each I/O slot occupies. DIP switch S3 1,2,and 3 determine which of the three positions is enabled. U-7 (74LS138) decodes 3 of the lower address lines to provide a select signal to each of the 8 I/O slots. U-1 and U-8 (8136) combine the upper address lines with VMA to provide an enable signal for the entire I/O block. The remaining low address lines A0, A1, and optionally A2 and A3 are routed to the I/O bus as RS0, RS1, RS2(UD-3) and RS3(UD-4).U-9 (74LS10) combines the enable signal from the address decoder with O2(E) clock and R/W from the buffers to provivide direction and enable control for Bi-directional buffers U-11 and U-12(74LS242) which control data flow between the main and I/O buses.The third section of U-9 drives one-shot U-10 (74121) to generate the 680x slow I/O signal.

BAUD RATE GENERATOR:

U-13 (14411) and crystal Y-1 form a standard bit rate generator. The outputs are connnected to J-1 where they can be jumpered to the input of U-14 (74L04) which buffers them and drives the baud rate lines on the I/O and, optionally, the main bus. DIP-switch S3-6(B) sets U-13 to one of two of its internal divide ratios.

GIMIX 6800/6809 MOTHERBOARD

PARTS LIST

QTY.	DESCRIPTION	LOCATION
2	8136	U-1,8
1	74LS240	U-2
# 3	74LS244	U-3,4,5
1	7805	U-6
1	74LS138	U-7
1	74LS10	U-9
1	74LS121	U-10
2	74LS242	U-11,12
1	14411	U-13
1	74L04	U-14
	# one standard two optional	
2	4.7K x 7 SIP	R-1,3
1	10 ohm	R-2
1	6.8K	R-4
1	4.7K	R-5
1	4.7K x 5 SIP	R-6
1	470 ohm	R-7
1	1.1K x 9 SIP	R-8
1	4.7K	R-9
3	6.8K	R-10,11,12
1	1M	R-20
8	10K no reference, soldered directly to back side of P.C. board.	
6	.047 uf ceramic	C-1,2,3,4,5,10
3	10 uf 25 V. tantalum	C-6,7,9
2	100 pf mica	C-8,11
1	2N3904 transistor	Q1
1	24-0034-9 P.C. board	
1	6107-14 heat sink	
2	6 position DIP-switch	S-1,2
1	5 position DIP-switch	S-3
99	MOLEX conn. # 09-70-1101 or equivalent.	
1	14 position barrier block	
1	4 position barrier block	
1	1.8432 Mhz. crystal	
4	DIP socket 20 pin	
3	DIP socket 16 pin	
6	DIP socket 14 pin	
1	DIP socket 24 pin	
1	DIP header 14 pin	
1	4-40 x 5/16 screw	
1	4-40 nut	

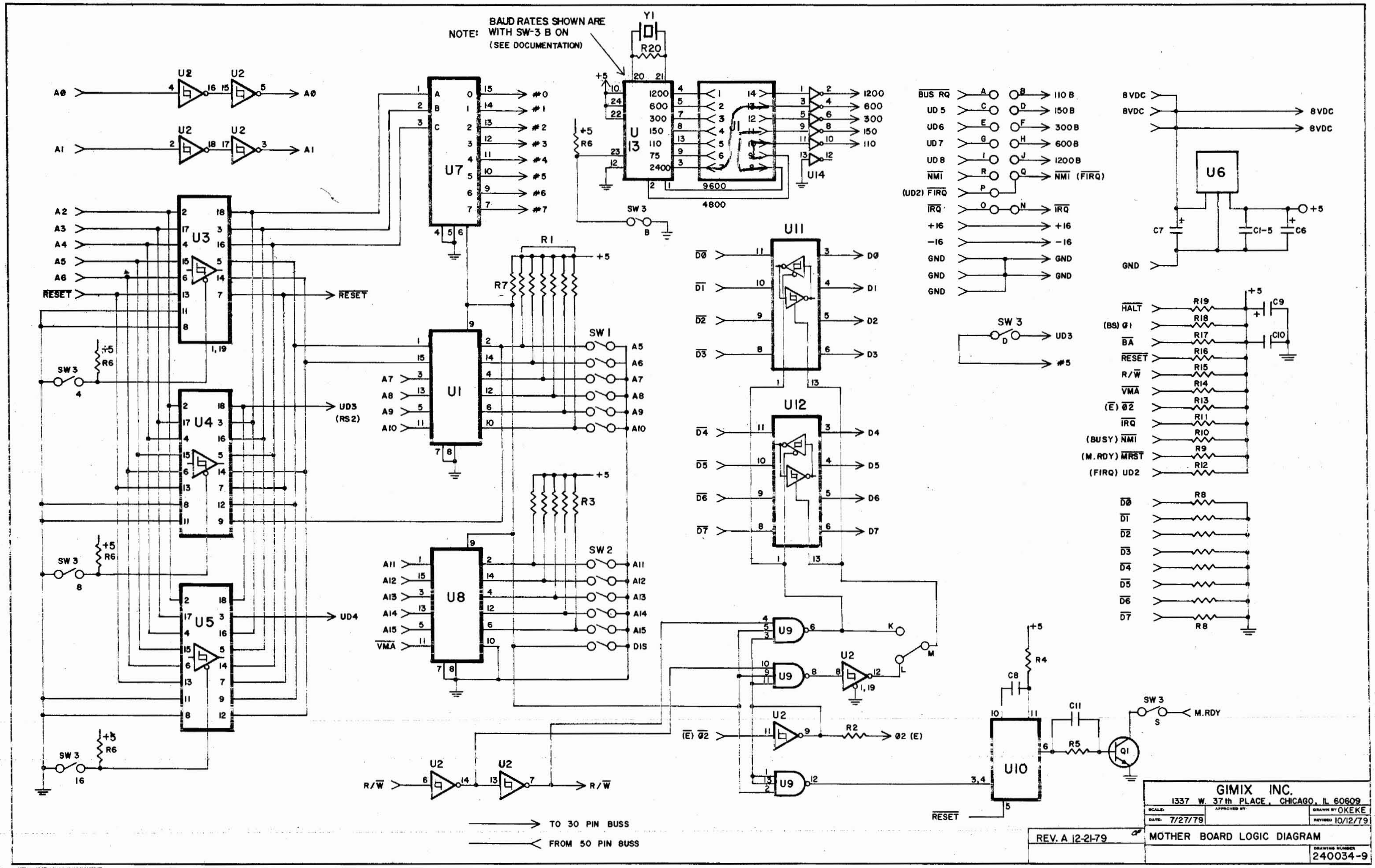
SS-50 BUS DESIGNATIONS

SS-50	GIMIX	SS-50C
D0	D0	D0
D1	D1	D1
D2	D2	D2
D3	D3	D3
D4	D4	D4
D5	D5	D5
D6	D6	D6
D7	D7	D7
A15	A15	A15
A14	A14	A14
A13	A13	A13
A12	A12	A12
A11	A11	A11
A10	A10	A10
A9	A9	A9
A8	A8	A8
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
GND	GND	GND
GND	GND	GND
GND	GND	GND
+8V	+8V	+8V
+8V	+8V	+8V
+8V	+8V	+8V
-12	-16	-16
+12	+16	+16
INDEX	INDEX	INDEX
MRST	MRDY	MRDY
NMI	NMI	BUSY
IRQ	IRQ	IRQ
UD2	FIRQ	FIRQ
UD1	Q	Q
02	E	E
VMA	VMA	VMA
R/W	R/W	R/W
RESET	RESET	RESET
BA	BA	BA
01	BS	BS
HALT	HALT	HALT
110b	BUSRQ	BUSRQ or 110b
150b	UD5	9600b or S3
300b	UD6	300b or S2
600b	UD7	4800b or S1
1200b	UD8	1200b or S0

SS-30	GIMIX	SS-30C
UD3	UD3	RS2
UD4	UD4	RS3
-12	-16	-16
+12	+16	+16
GND	GND	GND
GND	GND	GND
INDEX	INDEX	INDEX
NMI	FIRQ	FIRQ
IRQ	IRQ	IRQ
RS0	RS0	RS0
RS1	RS1	RS1
D0	D0	D0
D1	D1	D1
D2	D2	D2
D3	D3	D3
D4	D4	D4
D5	D5	D5
D6	D6	D6
D7	D7	D7
02	E	E
R/W	R/W	R/W
+8V	+8V	+8V
+8V	+8V	+8V
1200b	1200b	1200b
600b	600b	4800b
300b	300b	300b
150b	150b	9600b
110b	110b	110b
RESET	RESET	RESET
I/O SEL	CS	I/O SEL

NOTE: THIS CHART DOES NOT INDICATE THE POLARITY OF THE SIGNALS. IT IS ONLY A COMPARISON OF THEIR NAMES.

THE NAMES IN THE "GIMIX" COLUMN REFLECT THE DESIGNATIONS THAT APPEAR ON THE MOTHER BOARD ITSELF AND IN THE DOCUMENTATION. THE ACTUAL SIGNALS AT SOME OF THE PINS DEPENDS ON THE JUMPER CONFIGURATION OF THE BOARD AND THE PARTICULAR CPU CARD INSTALLED.


NOTE: BAUD RATES SHOWN ARE WITH SW-3 B ON (SEE DOCUMENTATION)
Y1
R20
U13
U1
U14
1200
600
300
150
110
75
2400
9600
4800
U2
U3
U4
U5
U7
U1
U8
U6
U9
U10
U11
U12
R1
R3
R7
R6
SW 1
SW 2
SW 3
A0
A1
A2
A3
A4
A5
A6
RESET
UD3 (RS2)
UD4
#0
#1
#2
#3
#4
#5
#6
#7
A7
A8
A9
A10
A11
A12
A13
A14
A15
VMA
DIS
BUS RQ
UD 5
UD6
UD7
UD 8
NMI
(UD2) FIRQ
IRQ
+16
-16
GND
110 B
150B
300B
600B
1200B
NMI (FIRQ)
8VDC
+5
C7
C1-5
C6
HALT
(BS) Ø1
BA
R/W
(E) Ø2
(BUSY) NMI
(M.RDY) MRST
(FIRQ) UD2
D0
D1
D2
D3
D4
D5
D6
D7
R19
R18
R17
R16
R15
R14
R13
R11
R10
R9
R12
R8
C9
C10
C8
C11
R4
R5
R2
Q1
M.RDY
Ø2 (E)
K
L
M
TO 30 PIN BUSS
FROM 50 PIN BUSS
GIMIX INC.
1337 W. 37th PLACE, CHICAGO, IL 60609
DRAWN BY OKEKE
DATE: 7/27/79
REVISED 10/12/79
REV. A 12-21-79
MOTHER BOARD LOGIC DIAGRAM
240034-9