

**Universal 2-Port Parallel
Interface Board**

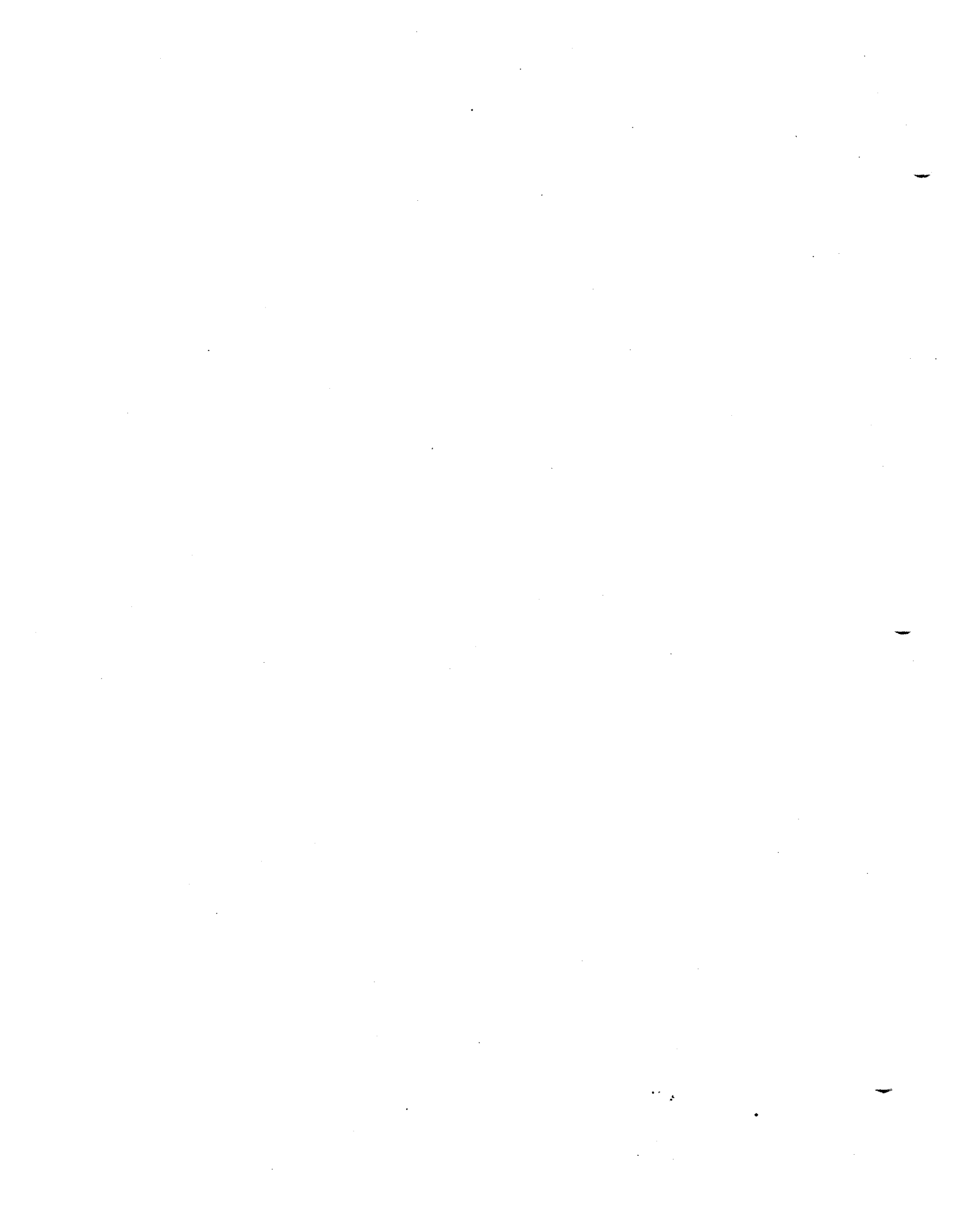
User's Manual

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GIMIX UNIVERSAL 2-PORT PARALLEL INTERFACE

FEATURES

- * 68B21 Parallel Interface Adapter (PIA)
- * Guaranteed 2Mhz. operation.
- * Two buffered, 8-bit bidirectional data ports.
- * Two buffered handshake lines (1 input and 1 bidirectional) per 8-bit port
- * Two 25-pin I/O connectors for compatibility with earlier GIMIX parallel interfaces.
- * Two 36-pin I/O connectors for easy connections to "Centronics" compatible parallel printers.
- * One 50-pin I/O connector for direct (unbuffered) access to all of the PIA I/O lines.
- * Occupies one 30-pin I/O slot in SS-50 bus systems

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INTRODUCTION

The GIMIX 2-PORT UNIVERSAL PARALLEL INTERFACE provides two 8-bit bidirectional data ports with handshake capabilities. Separate buffer control jumpers allow independent selection of input or output for each 8-bit port and for each port's bidirectional handshake line.

A variety of I/O connectors provide easy access to the ports. Each port has a 25-pin connector that is pinout compatible with the earlier GIMIX 2-port parallel interface. Each port also has a 36-pin connector that is pinout compatible with the "Centronics" type parallel printer interface. These connectors allow direct cabling to most parallel printers without the need to construct special cables. For special applications, a 50-pin connector provides direct (unbuffered) access to both ports. The 50-pin connector is pinout compatible with the WINDRUSH line of EPROM programmers. All five I/O connectors feature alternating signal and ground lines for maximum noise immunity.

SECTION 1: HARDWARE CONFIGURATION OPTIONS

The board has several options which may need to be properly configured before the board is used.

1-1: Buffer Disable Jumper (JA-1)

JA-1 enables or disables the I/O buffers for both 8-bit ports and their handshake lines. For normal, buffered operation, JA-1 must be in the enabled position (fig. C of the Jumper Options drawing). When JA-1 is placed in the disabled position (Fig. B), the outputs of ALL of the I/O buffers are placed in a high-impedance state. The disabled position should be selected when the 50-pin connector (P6) is used to connect an external device directly to the PIA.

1-2: 25-pin Connector, 5 Volt Option (JA-2, JA-10)

Jumper areas JA-2 and JA-10 provide the option of connecting the regulated +5 Volt supply from the board to pin 13 of I/O connectors P3 and P4 respectively. This option is provided for compatibility with earlier GIMIX 2-port parallel interfaces, and can be used to power an external device such as a keyboard. The board is normally supplied without jumpers at these locations. The option can be enabled by soldering a wire jumper between the pads at the appropriate jumper area. CAUTION: The board is capable of supplying approximately 200-300 ma. at 5 Volts to the external device(s). If the current requirements of the external device exceed this limit, improper operation and/or damage to the board may result.

1-3: Data Buffer Direction Option Jumper (JA-3, JA-11)

Jumper areas JA-3 and JA-11 control the direction of the buffers between the PIA data lines and the 25 and 36-pin I/O connectors. JA-3 selects the direction for the "B" side of the PIA (PBO-PB7) and JA-11 controls the "A" side (PA0-PA7). When a jumper is configured for OUTPUT (see fig. F of the Jumper Options drawing), the 8 data lines for the associated side of the PIA are buffered for data transfer from the PIA to the external device. When configured for INPUT (fig. G) the buffer direction is reversed. Note: These jumpers select the buffer direction for all 8 data bits of a port as a group. If simultaneous input and output from one 8-bit port, or program control of I/O direction is required, the buffers can not be used.

1-4: Handshake Buffer Direction Option Jumper (JA-4, JA-9)

Each "side" of the PIA has two associated handshake lines. One line [CA1(CB1)] is dedicated to input and its buffer is permanently set for input. The second handshake line [CA2(CB2)] can be programmed as an input or an output and its buffer direction is jumper selectable. JA-4 selects the buffer direction for the "B" side (CB2), JA-9 selects the direction for the "A" side (CA2). Figures I and J of the Jumper Options drawing show the configurations of JA-4 and JA-9 for input and output respectively.

1-5: 36-pin Connector, Grounding Options (JA-5, JA-7)

These jumpers provide the option of grounding or "floating" two of the pins (17 and 36) on the 36-pin I/O connectors, JA-5 for the "A"-side connector and JA-7 for the "B"-side. Pin 17 of the standard "Centronics" type interface is defined as CHASSIS or FRAME GROUND and is connected to the chassis of the printer mechanism. Pin 36 is defined as SELECT IN- (active low signal) and enables the printer when low. These pins are normally grounded by PC traces on the board, which can be cut to remove the ground from one or both pins. See the section on printer connections for more information.

1-6: RESET Output Option Jumpers (JA-6, JA-8)

One pin on each of the 26 and 36-pin I/O connectors can be used to connect the system RESET line from the 30-pin bus (buffered by the board) to the external device(s) connected to the board. This signal is normally high, and goes low on a RESET. JA-6 and JA-8 connect the input of the RESET buffers to either the system RESET line (see fig. M of the Jumper Options drawing) or to the 5 Volt supply (fig. N). See the section on printer connections for more information on the use of this option. JA-6 selects the desired option for the "B"-side connectors (P1 and P3), JA-8 is used for the "A"-side connectors (P2 and P4).

1-7: Interrupt Option Jumper (JA-12)

JA-12 is used to connect one or both of the interrupt outputs of the 6821 PIA to selected interrupt lines on the 30-pin bus. By appropriate selection of the jumpers, the interrupt outputs can be connected to either the IRQ or FIRQ/NMI lines on the bus. The choice of interrupts will depend on the operating system being used. For OS-9 or UniFLEX, the IRQ interrupt should be selected for both ports (or the selected port if only one is in use). FLEX does not use interrupts and, for FLEX only systems, the interrupts for both ports should be disabled. In OS-9/FLEX switching systems, interrupts must be enabled for proper operation of OS-9.

SECTION 2: EXTERNAL I/O CONNECTIONS

The board has five separate I/O connectors for making connections to external devices. The choice of connector(s) will depend on the particular application. The connectors used are standard .025" square pin headers on .100" centers. These connectors will mate with a variety of readily available "transition" connectors. Short cables with appropriate connectors, available separately from GIMIX, can be used to relocate the connectors to the back-panel of GIMIX mainframes for easy access.

2-1: 36-Pin Connectors (P1 and P2)

These connectors provide access to one 8-bit port per connector (P1 for the "B"-side and P2 for the "A"-side), with pinouts that match the standard "Centronics" type parallel printer interface. In addition to the required 8-bit data, DATA STROBE, and ACKNOWLEDGE signals, they provide options for connecting system RESET to the printers INIT- input (pin 31), connecting the printers CHASSIS GROUND (pin 17) to the system logic ground, and for enabling of the printer by grounding the printers SELECT IN- input (pin 36). All of the logic signals at this connector are fully buffered.

A transition cable, available from GIMIX, can be used to convert the 36-pin connectors on the board to back-panel mounted 36-pin female connectors of the type used on most "Centronics" compatible printers. A standard cable assembly, also available from GIMIX, can then be used to connect the printer to the computer.

For details of the connector pinout, see the Connector Pinout drawing.

2-2: 26-Pin Connectors (P3 and P4)

These connectors provide access to one 8-bit port per connector (P3 for the "B"-side and P4 for the "A"-side), with pinouts that match those used on earlier GIMIX 2-port parallel interfaces. These connectors provide access to 8 data lines, 2 handshake lines, system reset and regulated +5 Volts. NOTE: The earlier GIMIX 2-port parallel interface also provided regulated -12 Volts to the I/O connector, which is not available on this board. All of the logic signals at this connector are fully buffered.

A transition cable, available from GIMIX, can be used to convert the 26-pin connectors on the board to back-panel mounted 25-pin "D" type data connectors (DB25P).

For details of the connector pinout, see the Connector Pinout drawing.

2-3: Test Connector (P5)

This connector is provided for convenience during troubleshooting, and provides +5 V and ground for connecting logic probes, etc. It can also be used to provide power to external devices as long as the dissipation limits of the voltage regulator on the board are not exceeded.

2-4: 50-Pin Connector (P6)

This connector provides direct access (unbuffered) to all lines from both sides of the PIA. In addition, it provides access to the system RESET line (unbuffered), and all three UNREGULATED power supply voltages (+8, and +/- 16 Volts). The pinout of P6 matches the pinout of the WINDRUSH line of EPROM programmers and the board is used as the system interface for WINDRUSH PROGRAMMERS distributed by GIMIX.

This connector is useful in applications that require bidirectional use of some or all of the data lines on a particular port; the other (buffered) connectors can only be configured for 8-bits in or 8-bits out.

CAUTION: The power supply voltages available on P6 are UNREGULATED. Connection of these voltages (especially the -16 V) to the logic level signals on the board can damage the board and/or devices connected to it. If this connector is used to power external devices, proper regulation must be provided.

For details of the connector pinout, see the Connector Pinout drawing.

SECTION 3: 6821 PIA ADDRESSING

The 6821 requires 4 Bytes of address space. Since the board only decodes the lower 2 address lines, the PIA will appear more than once if the I/O slot decoding is set for more than 4 addresses per slot. The motherboards in all current GIMIX systems are configured for 16 addresses per slot, and the 6821 will appear 4 times within the slot's address space. Usually only the first (lowest) set of addresses is used. The following shows the location of the 4 PIA registers relative to the base address of the I/O slot.

Slot Address	PIA Register
Base+0	Peripheral Register/ Data Direction Reg. A
Base+1	Control Register A
Base+2	Peripheral Register/ Data Direction Reg. B
Base+3	Control Register B

SECTION 4: CONFIGURATIONS FOR SPECIFIC APPLICATIONS

4-1: Printer Configuration

Most of the available parallel interface printers use an interface standard developed by Centronics Data Corporation, Hudson, NH. This standard is commonly referred to as a "Centronics" interface. The pinouts used on the 36-pin connectors (P1 and P2) match a subset of the full interface standard and the pinouts of the connectors used on the printers. Most printers using this interface standard can be connected directly to the board with standard cables available from GIMIX. Note: The cable between the interface and printer should be as short as possible. Ten feet should be considered the maximum usable cable length.

GIMIX versions of the OS-9 and FLEX operating systems assume that the printer is connected to the "B" side of the interface in I/O slot #4. If only one printer is connected to the board, it will normally be connected to the "B" side (P1). A second printer can be connected to the "A" side; however, the user must make the appropriate modifications to the printer drivers (FLEX) or create a device descriptor (OS-9) to use the "A" side. Modifications to the software will also be needed if the board is installed in a different I/O slot. See the operating system documentation for more information.

The Data Buffer Direction Jumper for the selected side (JA-3 and/or JA-11) must be set for OUTPUT (fig. F of the Jumper Options Drawing). The Handshake Buffer Direction Jumper (JA-4 and/or JA-9) must also be set for OUTPUT (fig. J), and the buffers must be enabled by setting JA-1 to the ENABLED position (fig. C).

CAUTION: Before connecting a printer to the board, read the following information on optional connections and the printer manufacturer's documentation to determine the necessary options.

In addition to the data and handshake signals, several optional connections are also provided at P1(2).

PIN 17 of the printer interface is defined as CHASSIS or FRAME GROUND. This ground is normally the electrical protective ground, connected to the chassis of the printer. In many cases it is totally isolated from the logic or signal ground at the printer. PIN 17 is connected to logic ground on the GIMIX board through a PCB trace connecting two of the pads at JA-5 (for P1) and JA-7 (for P2). In most cases this pin can be left grounded; however, in certain instances, especially if the printer and computer are connected to different electrical outlets, this connection may result in ground loops and interfere with proper operation of the printer. Consult the printer manufacturer's documentation for information on grounding. The chassis and logic grounds can be isolated by cutting the appropriate PC trace(s) at JA-5 and/or JA-7.

PIN 31 of the printer interface is defined as INPUT PRIME or INIT. This line is usually an active low signal that resets the printer to its power-up state when pulled low. This pin can be made permanently high or connected to the system RESET line by JA-6 (for P1) and JA-8 (for P2). When the RESET option is selected, the printer will be

reset each time the system is reset. Check the printer manufacturer's documentation to determine the exact function of pin 31 and decide which option best suits the application.

PIN 36 of the printer interface is defined as SELECT IN. This is usually an active low signal that enables the printer. For some printers, this line must be pulled low by the interface to enable printing. PIN 36 is connected to logic ground on the GIMIX board through a PCB trace connecting two of the pads at JA-5 (for P1) and JA-7 (for P2). Check the printer manufacturer's documentation to determine the exact function of pin 36 for the printer being used. PIN 36 can be isolated from ground if necessary, by cutting the appropriate PC trace(s) at JA-5 and/or JA-7.

The following table summarizes the board configuration required for parallel printers.

Jumper Option		Configuration	Figure
"B"-Side	"A"-Side		
JA-1	JA-1	Buffers enabled	C
JA-2	JA-10	Don't Care	
JA-3	JA-11	Output	F
JA-4	JA-9	Output	J
JA-5	JA-7	See text	
JA-6	JA-8	See text	
JA-12	JA-12	As required by operating system	

4-2: Windrush EPROM Programmer Configuration

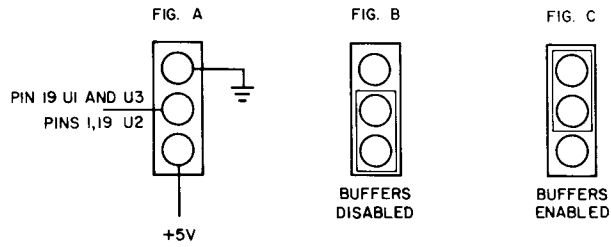
The following table summarizes the required board configuration for use with the Windrush EPROM programmers distributed by GIMIX. In this application the board is used in the unbuffered mode, and the programmer connects to both ports through 50-pin I/O connector P6. To minimize loading on the PIA, the buffers are disabled and set to the INPUT configuration. For OS-9, both sides of the PIA must have IRQ interrupts enabled; for FLEX, interrupts should be disabled.

Jumper Option		Configuration	Figure
"B"-Side	"A"-Side		
JA-1	JA-1	Buffers disabled	B
JA-2	JA-10	Don't Care	
JA-3	JA-11	Input	G
JA-4	JA-9	Input	I
JA-5	JA-7	Don't care	
JA-6	JA-8	Reset disabled	N
JA-12	JA-12	See above	

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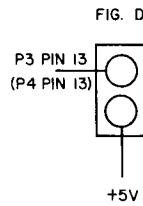
JA-1

BUFFER DISABLE OPTION



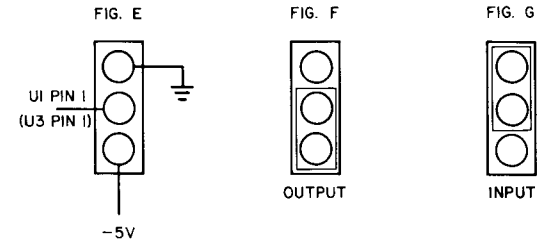
JA-2 (JA-10)

P3 (P4) +5 VOLT OPTION



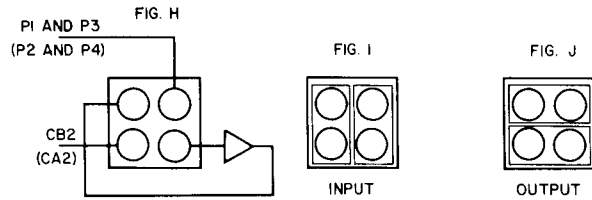
JA-3 (JA-11)

BUFFER DIRECTION OPTION



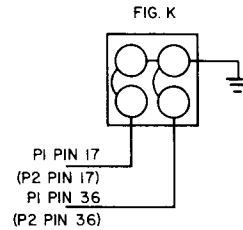
JA-4 (JA-9)

HANDSHAKE BUFFER DIRECTION OPTION



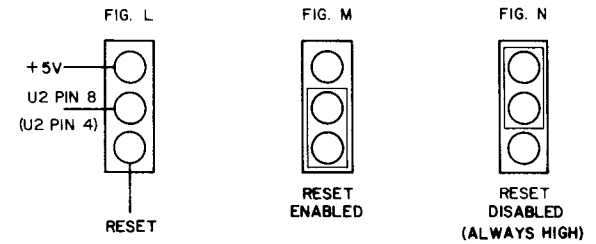
JA-5 (JA-7)

36-PIN CONNECTOR
GROUNDING OPTIONS



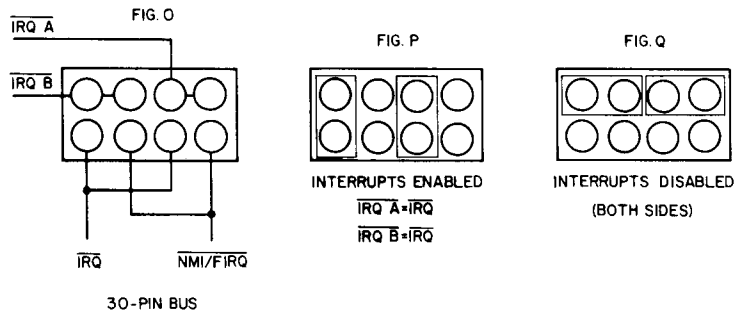
JA-6 (JA-8)

RESET OUTPUT OPTION



JA-12

INTERRUPT OPTIONS



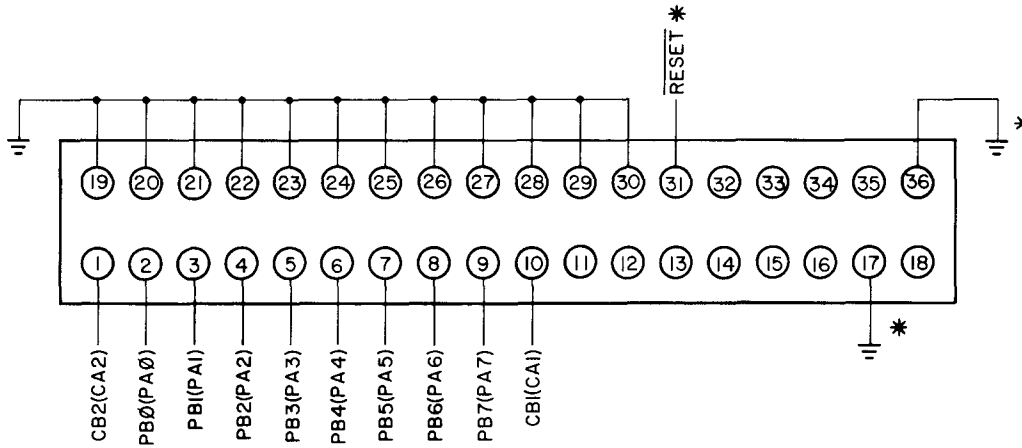
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1337 W. 37th PL. CHICAGO, IL 60609	
6-7-84	DRAWN BY: CLARK PETROUSEK
UNIVERSAL PARALLEL INTERFACE JUMPER OPTIONS DRAWING	
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NOTES:

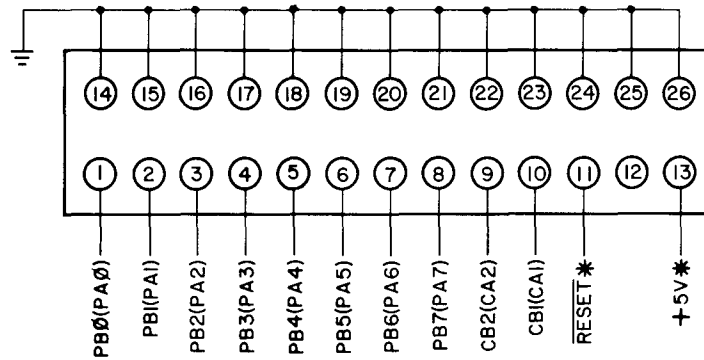
* JUMPER OPTIONS

1. DESIGNATIONS IN PARENTHESIS ARE FOR THE "A" SIDE.
2. ALL UNLABELED PINS ARE UNCONNECTED.
3. CONNECTORS SHOW FROM COMPONENT SIDE OF CIRCUIT BOARD.
4. PINOUTS APPLY TO THE CONNECTORS ON THE BOARD AND TO THE RIBBON CABLE CONNECTORS WHEN GIMIX BACKPANEL CABLES ARE USED.

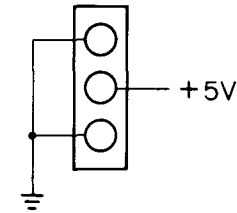
PI(P2)



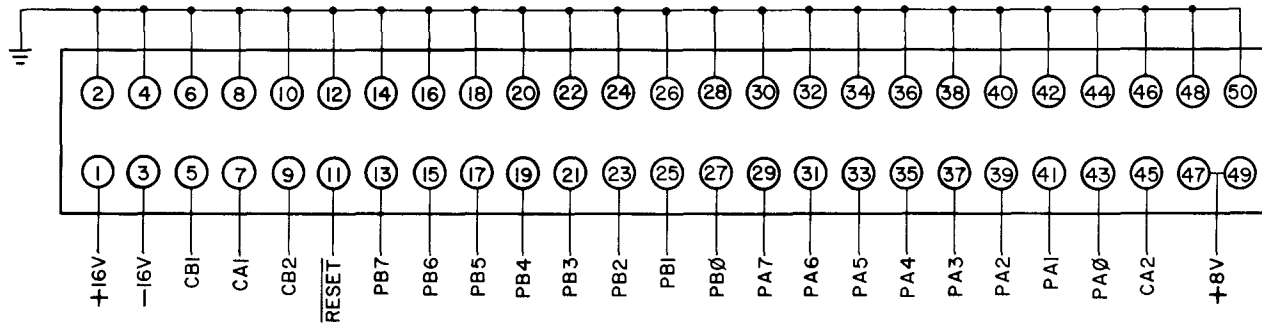
P3(P4)



P5

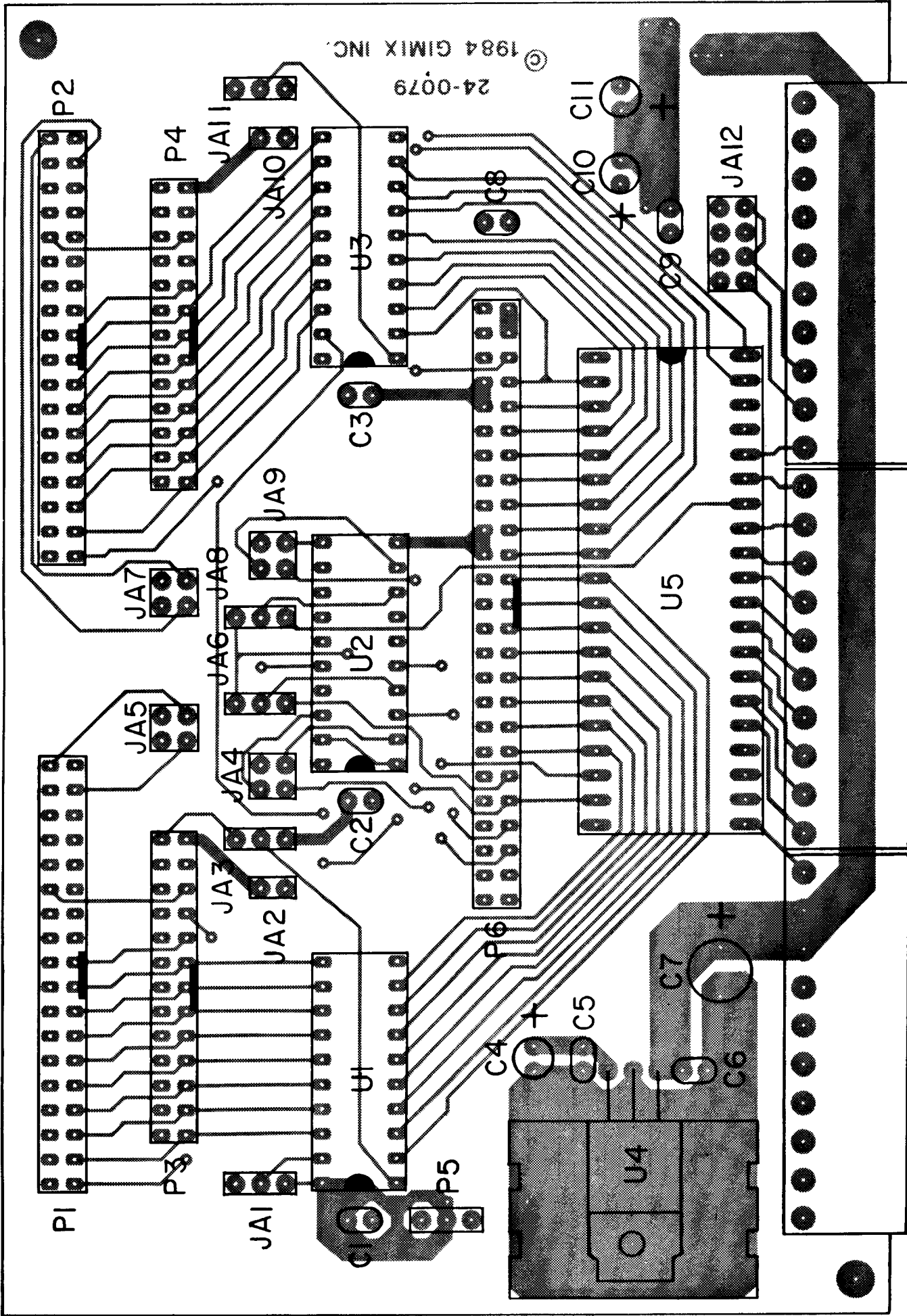


P6



GIMIX INC. 1337 W. 37th PL. CHICAGO, IL. 60609	
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COMPONENT LAYOUT

